

1      **ABSTRACT OF THE DISCLOSURE**

2      The invention includes a number of methods and structures pertaining  
3      to semiconductor circuit technology, including: methods of forming DRAM  
4      memory cell constructions; methods of forming capacitor constructions; DRAM  
5      memory cell constructions; capacitor constructions; and monolithic integrated  
6      circuitry. The invention includes a method of forming a capacitor comprising  
7      the following steps: a) forming a mass of silicon material over a node  
8      location, the mass comprising exposed doped silicon and exposed undoped  
9      silicon; b) substantially selectively forming rugged polysilicon from the exposed  
10     undoped silicon and not from the exposed doped silicon; and c) forming a  
11     capacitor dielectric layer and a complementary capacitor plate proximate the  
12     rugged polysilicon and doped silicon. The invention also includes a capacitor  
13     comprising: a) a first capacitor plate; b) a second capacitor plate; c) a  
14     capacitor dielectric layer intermediate the first and second capacitor plates; and  
15     d) at least one of the first and second capacitor plates comprising a surface  
16     against the capacitor dielectric layer and wherein said surface comprises both  
17     doped rugged polysilicon and doped non-rugged polysilicon.

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